SYSTOLIC ARRAY ARCHITECTURE AND ITS APPLICATION IN FINITE IMPULSE RESPONSE FILTER DESIGN

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ABSTRACT

This project presents the methodology involved in mapping a computing algorithm onto Systolic Array (SA) architecture and its implementation in designing a high computational throughput Finite Impulse Response (FIR) filter. As in many applications of Digital Signal Processing (DSP), FIR filtering requires enormous computing power, especially for applications in real-time environment where fast computations of data is demanded. Fortunately, the FIR filter algorithm is a compute-bound computation, and speeding up this computation can be achieved through systolic approach. Prior to designing the SA FIR filter hardware module in Quartus II, the FIR filter was first designed and analyzed via MATLAB to obtain the filter coefficients and simulation results needed in hardware design. Verification and performance analyses of the SA FIR filter were done based on both simulation results from MATLAB and hardware designs. Simulation result of the SA FIR filter proved the capability of SA architecture to produce high computational throughput, but at the expense of a large number of resources. In addition, the simulation results displayed some limitations of this particular design in terms of its response time and accuracy of the results. Thus, improvements of the design have been proposed to increase its performance.

ABSTRAK

Projek ini mempersembahkan kaedah yang terlibat dalam pemetan algorithma pengiraan ke seni bina sistolik dan aplikasinya dalam reka bentuk penapis sambutan dedenyut terhingga. Seperti dalam banyak aplikasi pemprosesan isyarat digital, proses penapisan sambutan dedenyut terhingga memerlukan kuasa pengiraan yang sangat besar, terutamanya untuk aplikasi dalam persekitaran masa sebenar di mana pengiraan data yang pantas diperlukan. Mujurlah, jumlah operasi pengiraan yang terlibat dalam penapisan sambutan dedenyut terhingga melebihi jumlah elemen input dan output. Oleh itu, pengiraan yang pantas boleh dicapai melalui pendekatan sistolik. Sebelum penapis sambutan dedenyut terhingga dalam seni bina systolik direka bentuk menerusi perisian Quartus II, penapis tersebut telah terlebih dahulu direka bentuk dan dianalisis melalui perisian MATLAB untuk mendapatkan pekali penapis dan keputusan simulasi yang diperlukan. Pengesahan dan analisis prestasi penapis sambutan dedenyut terhingga dalam seni bina sistolik telah dilakukan berdasarkan kedua-dua keputusan simulasi dari perisian MATLAB dan Quartus II. Hasil simulasi penapis sambutan dedenyut terhingga dalam seni bina sistolik membuktikan keupayaan seni bina sistolik untuk pengiraan data yang pantas, tetapi memerlukan jumlah sumber peranti yang tinggi. Di samping itu, keputusan simulasi juga memaparkan beberapa batasan terhadap reka bentuk ini khususnya dari segi masa tindak balas dan kejituan pengiraan. Oleh itu, penambahbaikan reka bentuk telah dicadangkan untuk meningkatkan prestasi penapis.

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LIST OF ABBREVIATIONS

CU	-	Controller Unit
DG	-	Dependence Graph
DSP	-	Digital Signal Processing
DU	-	Data Path Unit
FIR	-	Finite Impulse Response
FPGA	-	Field-Programmable Gate Array
HDL	-	Hardware Description Language
I/O	-	Input/Output
IIR	-	Infinite Impulse Response
MAC	-	Multiplier-Accumulator
PEs	-	Processing Elements
SA	-	Systolic Array
SFG	-	Signal Flow Graph
RTL	-	Register-Transfer Level
VLSI	-	Very Large Scale Integrated Circuit

CHAPTER 1

INTRODUCTION

This report presents the methodology involved in mapping a computing algorithm onto Systolic Array (SA) architecture and its implementation in Finite Impulse Response (FIR) filter design. This chapter discusses the rationales of the project, project objectives, scope of work and report organization.

1.1 Project Rationales and Objectives

Digital Signal Processing (DSP) involves enormous computing power, especially for applications in real time environment where fast computations of data is required. Computational tasks can be generally classified into two; compute-bound computations and Input/Output (I/O)-bound computations. In a computation, if the total number of operations is larger than the total number of input and output elements, then the computation is compute-bound, otherwise it is I/O-bound. Any attempt to speed up an I/O-bound computation must rely on an increase in memory bandwidth. Speeding up a compute-bound computation, however, may be

accomplished in a relatively simple and less expensive manner, that is, by systolic approach.

Thus, the main objective of this project is to study and analyze the methodology involved in mapping a computing algorithm onto SA architecture on Field-Programmable Gate Array (FPGA). The other objective is to implement the methodology in designing a high computational throughput SA FIR filter.

1.2 Scope of Work

SA of the FIR filter was developed based on three main references; Why Systolic Architecture? by H. T. Kung, VLSI Array Processors: Design and Applications by S. Y. Kung, and Methodology for Mapping Algorithm onto Systolic Array Architecture in its Application on Matrix-Vector Multiplication Algorithm by Nordinah Ismail.

MATLAB software was used to initially design, analyze and obtain important design specifications of the FIR filter. Altera Quartus II design tool and Verilog Hardware Description Language (HDL) were utilized for hardware design and analysis. Simulation results from MATLAB and hardware designs were compared for verification and analysis of the SA FIR filter.

1.3 Report Organization

This report is organized into six chapters. Chapter 1 discusses the rationales of the project, project objectives, scope of work and report organization.

Chapter 2 gives an overview and theoretical background of SA architecture and FIR filter. Some design examples of SA architecture are discussed as well.

Chapter 3 describes the methodology of the project. The SA FIR filter design steps are also introduced in this chapter.

Chapter 4 and 5 present the MATLAB and hardware designs and analyses of the SA FIR filter. The MATLAB and hardware design steps are discussed in detail in these chapters.

Chapter 6 concludes the findings of the project and proposes potential future work for design improvement.

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